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Programming

Conquering Noise with Hardware Counters on HPC Systems

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EXTRA NOISE

Motivation



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Performance and complexity of HPC systems are constantly increasing

- → Important to examine the scaling behavior of an application and identify performance bottlenecks early
- → Use empirical performance modeling (e.g., Extra-P)

Problem:

In **noisy** environments \rightarrow difficult to create accurate performance models

- Strong run-to-run variations of the underlying measurements
- Irreproducible and misleading
- Deviation from *intrinsic* application behavior

Empirical performance modeling

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Performance measurements with different execution parameters $x_1,...,x_n$







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Problem (cont.):

- Application runtime affected by noise
 - Most common performance metric



Solution:

Use hardware counters

- Noise has little impact on some hardware counters
 - E.g., floating-point operations
- Selecting the right counters requires a thorough analysis
- Once found, the counters can be used for performance modeling

Contributions



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A detailed noise analysis on various hardware counters on different systems:

→ Total of **26950** experiments (**PAPI preset** events only):

3-	Five systems		With and without injected noise
<u></u>	Four hardware architectures		Multiple resource configurations (number of nodes)
	Three applications	G	Five repetitions per setup

Categorized the counters across the different systems according to their noise resilience and provided a **user guide**

Analysis Methodology



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Find noise-resilient hardware counters:

- Examine if counters' values change when repeating the measurements
- Expose the counters to different levels of noise
 - Using NOIGENA (NOIse GENerator Application) developed in Jülich
 - NOIGENA processes were running on the odd processors
 - Inject different noise patterns using NOIGENA

NOIse GENerator Application

- Produces shared-resource contention
- Uses several benchmarks
 - Memory: Stream
 - Network: FzjLinkTest
 - I/O: IOR
- Consecutively runs configurable patterns

PATTERN_1:			
Sequence:			
- REPEATED_NOISE:			
REPEAT: inf			
Sequence:			
- NETWORK_NOISE: 2			
- NO_NOISE: 2			
- MEMORY_NOISE: 2			
- NO_NOISE: 2			

Noise pattern used by NOIGENA to configure the amount and duration of generated noise.



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Analysis Methodology



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- Instrument all call paths of the applications with Score-P using PAPI
- We do the analysis for each counter, on all systems, with and without injected noise to get the Score-P measurements for the:
 - *a*th application kernel (call path),
 - *p*th MPI rank,
 - tth OpenMP thread, and
 - *i*th repetition:



a counter value $v_{a,p,t,i}$

Analysis Methodology



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Compare counter values across the **repeated experiments** for each a^{th} application kernel (call path), p^{th} MPI rank, and t^{th} OpenMP thread

• Find the **arithmetic mean** across the repetitions:

 $\bar{v}_{a,p,t} = \text{mean}(v_{a,p,t,i})$

• Calculate the **relative deviation from the arithmetic mean** in percent:

$$\frac{\left|v_{a,p,t,i}-\bar{v}_{a,p,t}\right|}{\bar{v}_{a,p,t}}*100\%$$

 \rightarrow Use this metric to compare the counter results

Application Benchmarks





For all of them, we used OpenMP and MPI for the measurements

Evaluation Systems



Alias	Name	Nodes	Processor	RAM	Network
СМ	DEEP-EST, Cluster Module	50	2x Intel Xeon Skylake Gold 6146 CPUs (12 cores, 24 threads)	192 GB DDR4 RAM (2666 MHz)	InfiniBand EDR (100 GBit/s)
ESB	DEEP-EST, Extreme Scale Booster	75	1x Intel Xeon Cascade Lake Silver 4215 CPU (8 cores, 16 threads)	48 GB DDR4 RAM (2400 MHz),	InfiniBand EDR (100 GBit/s)
Jureca	JURECA DC Module, std. compute nodes	480	2x AMD EPYC 7742 CPUs (64 cores, 128 threads)	512 GB DDR4 RAM (3200 MHz)	InfiniBand HDR100 (100 GBit/s)
Jetson	OACISS, Franken-cluster Jetson ARM64	12x Jetson Tegra TX1	1x Quad-Core ARM Cortex®- A57 MPCore (4 cores, 4 threads)	4 GB 64-bit LPDDR4 RAM	1 GBit/s ethernet
Cyclops	OACISS, Franken-cluster Cyclops	1	2x 20c IBM Power9 CPUs (20 cores, 80 threads)	384 GB of RAM	BNX2 10G Ethernet NICs, 2x Infiniband EDR (25 GBit/s)

Application Configurations



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App	System	Experiment configuration
MiniFE	СМ	$n = [1, 2, 4, 8], p = n, t = 12p, s = 20^3 p$
	ESB	$n = [1, 2, 4, 8, 12, 16, 32], p = n, t = 8p, s = 50^3 p$
	Jureca	$n = [4, 8, 12, 16, 20, 24], p = n, t = 128p, s = 20^3 p$
	Jetson	$n = [2, 3, 4, 5, 6], p = n$, $t = 2p, s = 50^3 p$
	Cyclops	$n = 1, p = [4, 8, 12, 16, 20], t = 4p, s \approx 24^3 p$
HS	СМ	$n = [1, 8, 27], p = n, t = 12p, s = 10^3 p$
	ESB	$n = [1, 8, 27], p = n, t = 8p, s = 30^3 p$
LE	Jureca	$n = [1, 8, 27], p = n, t = 128p, s = 10^3 p$
ΓN	Jetson	$n = 8, p = n, t = 2p, s = 15^3 p$
	Cyclops	$n = 1, p = [1, 8, 27, 64], t = p, s = 5^3 p$
LAMMPS	СМ	$n = [1, 2, 4, 8], p = n, t = 12p, s = 20^{3}p$
	ESB	$n = [1, 2, 4, 8, 12, 16, 32], p = n, t = 8p, s = 20^3 p$
	Jureca	$n = [1, 2, 4, 8, 16], p = n, t = 128p, s = 20^3 p$
	Jetson	$n = [2, 3, 4, 5, 6], p = n, t = 2p, s = 20^3 p$
	Cyclops	$n = 1, p = [4, 8, 12, 16, 20], t = 4p, s = 20^3 p$

s: problem size n: number of computational nodes p: the number of MPI processes t: the number of OpenMP thread

Evaluation Results



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Visualizing the results for **each counter** is not an easy task:



To compare distinct counter \rightarrow Scale the plots with the peak occurrence of the relative deviation

Evaluation Results

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- Height = how often the corresponding relative deviation occurs
- Intensity = share of the total counter value for that call path (importance)
- Only call paths with > 1% of the total counter value are visible



Evaluation Results: How to Interpret the Results



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Bad Counters [X]

Counter strongly influenced by noise:

 Large distribution in the presence of noise, small one in the absence Counter with large deviation:

- Large distribution disregarding the noise
- Not suited for modeling



Evaluation Results: How to Interpret the Results



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Good Counters [+]

Counter robust against noise:

- Similar distribution in the presence and absence of noise
- Small deviation (< 20%)</p>



OK Counters [0]

Counter to some extent robust against noise:

- Small deviation (< 20%) without noise</p>
- Small deviation (< 20%) in the presence of</p> noise for significant call paths

Evaluation Results: Runtime







Evaluation Results: Floating Point Operations

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Evaluation Results: Instructions, Cycles

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Evaluation Results: Instructions, Cycles





Evaluation Results: L1, L2 Instruction Cache



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Evaluation Results: Stalls & Reference Cycles





Evaluation Results: L2, L3 Cache





Impact of the Application: Time and Load Inst.



LAMMPS

LULESH

MiniFE



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Best Practice User Guide





	Jureca (AMD)	ESB (Intel)	CM (Intel)	Jetson (ARM)	Cyclops (IBM)
Floating point ops./instr.	++	++	++	++	++
Cycles	×	+	+	0	0
Instructions	×	+	+	+	+
L1	+	X	×	0	+
L2	+	0	X	0	+
L3		X	X		X

Legend		
++	very good	
+	good	
0	ok	
X	bad	

Conclusion



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- Examined noise resilience of hardware counters on five systems with different architectures (Intel, AMD, ARM, IBM Power9)
- Analyzed all available presets and a selection of native events
- Most hardware counters are affected by noise, but still less than the runtime
- Floating-point operations or instructions are noise resilient on all systems
- Variability significantly depends on the system architecture
- Best practice guide helps choose suitable counters for given system



Marcus Ritter, Ahmad Tarraf, Alexander Geiß, Nour Daoud, Bernd Mohr, Felix Wolf: Conquering Noise With Hardware Counters on HPC Systems. In Proc. of the Workshop on Programming and Performance Visualization Tools (ProTools), held in conjunction with the Supercomputing Conference (SC22), pages 1–10, IEEE, 2022.

Future Work

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- Create a tool that performs the analysis and evaluation on the system
- Examine more counters (i.e., native counters)
- Examine the correlation between the counters
- Identify the source of variation
- Started working with the PAPI developers











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Questions?

Thank you for your attention!

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